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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 06/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/716,378	MINE, KAZUMASA	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *07 December 2004 and 21 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19-23* is/are allowed.

6)☒ Claim(s) *1-18 and 24-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-23 and new claims 24-35 have been considered. Claims 1, 16, 19, and 22 have been amended as per Applicant's request. New claims 24-35 have been added per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: RCE as received on 07 December 2004; Amendment as received on 07 December 2004; Extension of Time 3 Months as received on 07 December 2004; Change of Address as received on 22 December 2004; and Amendment as received on 21 April 2005.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 24 are rejected under 35 U.S.C. 102(e) as being taught by Levy, U.S. Patent Number 5,923,892 (herein referred to as Levy).

6. Referring to claim 24, Levy has taught a microprocessor system for executing instructions described in a program comprising:

a. A main processor for executing by hardware those instructions which belong to a first instruction set (Levy Abstract; column 2, lines 49-63; Figure 2; and Figure 3) and for executing by software those instructions which belong to a second instruction set (Levy Abstract; column 9, lines 46-59; column 10, lines 4-36; Figure 2; and Figure 3); and

b. A co-processor operative under the control of said main processor for autonomously fetching an instruction belonging to said second instruction set to execute the fetched instruction by hardware of the co-processor (Levy Abstract; column 2, lines 35-63; column 8, lines 34-41; column 9, lines 42-46; Figure 2; and Figure 3),

c. Wherein said coprocessor is provided with:

i. A stack memory for holding data generated in the course of execution of an instruction which belongs to said second instruction set (Levy Abstract; column 7, lines 61-64; column 11, lines 1-14; and Figure 3);

ii. A stack pointer for holding an address of the most recent data in said stack memory (Levy column 5, lines 18-42; column 7, lines 29-42; Figure 3; and Figures 8-12);

iii. A program counter for holding an address of an instruction which is currently processed and belongs to said second instruction set (Levy column 5, lines 18-42; column 7, lines 29-42; column 9, lines 42-46; Figure 3; Figure 6; and Figure 7); and

iv. An updating circuit for, in response to the detection of an encounter with a specific instruction among instructions belonging to said second instruction set for which data presently under the control of said main processor needs to be (Levy Abstract; column 6, line 50 to column 7, line 24; Figure 6; and Figure 7), issuing a notification of said encounter to said main processor to request the main processor to execute said specific instruction (Levy Abstract; column 6, line 50 to column 7, line 24; Figure 6; and Figure 7), and for updating said stack pointer in said stack memory and said program counter (Levy column 5, lines 18-42; column 7, lines 29-42; column 9, lines 42-46; Figure 3; Figure 6; and Figure 7).

7. Referring to claim 26, Levy has taught wherein said co-processor comprises a status register for holding information indicative of a need of said notification and wherein said main processor periodically accesses said status register to recognize that said co-processor has encountered said specific instruction to thereby execute said specific instruction (Levy column 5, lines 18-42; column 7, lines 29-64; column 8, lines 21-24; Figure 3; Figure 6; and Figure 7).

8. Referring to claims 28, 29, and 31, Levy has taught

a. Wherein said main processor refers to and instruction queue of said co-processor to specify an interrupt handler which corresponds to said specific instruction to be

executed (Applicant's claim 28) (Levy column 9, lines 42-59; Figure 6; and Figure 7);

b. Wherein said co-processor includes a stack architecture (Applicant's claim 29) (Levy Abstract; column 5, lines 31-59; and Figure 3);

c. A stack-top register for holding a predetermined number of top data of stack data (Applicant's claim 31) (Levy column 5, lines 18-42; column 7, lines 29-42; Figure 3; and Figures 8-12); and

d. A cache memory provided between said stack memory and said stacktop register for caching a part of data held in said stack memory (Applicant's claim 31) (Levy column 11, lines 1-14; Figure 3; and Figure 10).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1, 2, 4-16, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levy, U.S. Patent Number 5,923,892 (herein referred to as Levy) in view of Holmbo, U.S. Patent Number 4,860,200 (herein referred to as Holmbo).

11. Referring to claim 1, Levy has taught a microprocessor system for executing instructions described in a program comprising:

a. A main processor for executing, by hardware, instructions which belong to a first instruction set (Levy Abstract; column 2, lines 49-63; Figure 2; and Figure 3) and

for executing, by software, instructions which belong to a second instruction set (Levy Abstract; column 9, lines 46-59; column 10, lines 4-36; Figure 2; and Figure 3); and

b. Said main processor including an interrupt request reception circuit (Levy Abstract; column 6, line 50 to column 7, line 24; Figure 6; and Figure 7);

c. A co-processor operative under the control of said main processor for autonomously fetching an instruction belonging to said second instruction set to execute same by hardware of said co-processor, (Levy Abstract; column 2, lines 35-63; column 8, lines 34-41; column 9, lines 42-46; Figure 2; and Figure 3);

d. Said co-processor including an interrupt request generation circuit, said interrupts request generation circuit being connected to said interrupt request reception circuit by at least one signal line and allowing an interrupt address to be identified in said main processor (Levy column 8, lines 21-24; column 9, lines 46-59; column 10, lines 4-36; Figure 3; Figure 6; and Figure 7).

12. Levy has not taught

a. To decode an interrupt vector for said execution of an instruction of said second instruction set by using an interrupt handler; and

b. Encoding said interrupt vector.

13. Holmbo has taught

a. To decode an interrupt vector for said execution of an instruction of said second instruction set by using an interrupt handler(Holmbo Abstract; column 2, lines 11-21 and 43-58; column 3, lines 4-8, 30-43, and 60-67; and Figure 2); and

b. Encoding said interrupt vector(Holmbo Abstract; column 2, lines 11-21 and 43-58; column 3, lines 4-8, 30-43, and 60-67; and Figure 2).

14. A person of ordinary skill in the art at the time the invention was made, and as taught by Holmbo, would have recognized that using vector interrupts decreases the delay caused by executing an interrupt (Holmbo column 2, lines 6-8), thereby increasing the speed and efficiency of interrupt execution. In regards to Holmbo, Holmbo has taught in the cited lines that executing an interrupt in the additional peripheral device that does not use interrupt vectors like the processor in Holmbo's device causes a delay in executing the interrupt routine. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the interrupt vectors of Holmbo in the device of Levy to increase the speed and efficiency of interrupt execution.

15. Referring to claim 2, Levy has taught wherein said co-processor detects an encounter with a specific one of the instructions belonging to said second instruction set which said co-processor cannot process by itself and issues a notification of said encounter to said main processor to thereby request the main processor to execute said specific instruction (Levy Abstract; column 9, lines 46-59; column 10 ,lines 4-36; Figure 2; Figure 3; Figure 6; and Figure 7).

16. Referring to claims 4-7 and 11, Levy has taught:

a. Wherein said co-processor issues said notification by dedicated interrupt assigned in advance respectively to a predetermined number of the instructions belonging to said second instruction set which have a higher frequency of execution than the

other instructions (Applicant's claims 4) (Levy Abstract; column 6, line 50 to column 7, line 24; Figure 6; and Figure 7)

b. Wherein said interrupt request reception circuit in said main processor encodes said dedicated interrupts sent from said co-processor (Applicant's claim 11) (Levy column 8, lines 21-24; column 9, lines 46-59; column 10, lines 4-36; Figure 3; Figure 6; and Figure 7).

17. Levy has not taught:

a. Interrupt vectors (Applicant's claim 4)

b. Wherein at least one of said dedicated interrupt vectors is assigned to a plurality of instructions belonging to said second instruction set (Applicant's claim 5)

c. Wherein priorities are set to a plurality of said dedicated interrupt vectors (Applicant's claim 6)

d. Wherein a single instruction is assigned to a given one of said dedicated interrupt vectors to which a higher priority is set, while a plurality of instructions are assigned to a given one of said dedicated interrupt vectors to which a lower priority is set (Applicant's claim 7)

e. Specify an interrupt handler which corresponds to said specific instruction to be processed (Applicant's claim 11).

18. Holmbo has taught:

a. Interrupt vectors (Applicant's claim 4) (Holmbo Abstract; column 2, lines 11-21 and 43-58; column 3, lines 4-8, 30-43, and 60-67; and Figure 2)

b. Wherein at least one of said dedicated interrupt vectors is assigned to a plurality of instructions belonging to said second instruction set (Applicant's claim 5) (Holmbo Abstract; column 2, lines 11-21 and 43-58; column 3, lines 4-8, 30-43, and 60-67; and Figure 2). In regards to Holmbo, the interrupts react to interrupts that are occurring due to certain instructions in Holmbo's additional peripheral device.

c. Wherein priorities are set to a plurality of said dedicated interrupt vectors (Applicant's claim 6) (Holmbo Abstract; column 2, lines 11-21 and 43-58; column 3, lines 4-8, 30-43, and 60-67; and Figure 2);

d. Wherein a single instruction is assigned to a given one of said dedicated interrupt vectors to which a higher priority is set, while a plurality of instructions are assigned to a given one of said dedicated interrupt vectors to which a lower priority is set (Applicant's claim 7) (Holmbo Abstract; column 2, lines 11-21 and 43-58; column 3, lines 4-8, 30-43, and 60-67; and Figure 2); and

e. Specify an interrupt handler which corresponds to said specific instruction to be processed (Applicant's claim 11) (Holmbo Abstract; column 2, lines 11-21 and 43-58; column 3, lines 4-8, 30-43, and 60-67; and Figure 2).

19. A person of ordinary skill in the art at the time the invention was made, and as taught by Holmbo, would have recognized that using vector interrupts decreases the delay caused by executing an interrupt (Holmbo column 2, lines 6-8), thereby increasing the speed and efficiency of interrupt execution. In regards to Holmbo, Holmbo has taught in the cited lines that executing an interrupt in the additional peripheral device that does not use interrupt vectors like the

processor in Holmbo's device causes a delay in executing the interrupt routine. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the interrupt vectors of Holmbo in the device of Levy to increase the speed and efficiency of interrupt execution.

20. Referring to claims 8-10, Levy has taught wherein said co-processor further comprises:

a. A stack memory for holding data generated in the course of execution of an instruction which belongs to said second instruction set (Applicant's claim 8) (Levy Abstract; column 7, lines 61-64; column 11, lines 1-14; and Figure 3);

b. A stack pointer for holding an address of the most recent data in said stack memory (Applicant's claim 8) (Levy column 5, lines 18-42; column 7, lines 29-42; Figure 3; and Figures 8-12);

c. A hardware resource for carrying out a process for updating said stack pointer among processes which take place in the course of execution of said specific instruction (Applicant's claim 8) (Levy column 12, lines 26-31 and Figures 8-12);

d. A program counter for holding an address of an instruction which is currently processed and belongs to said second instruction set (Applicant's claim 9) (Levy column 5, lines 18-42; column 7, lines 29-42; column 9, lines 42-46; Figure 3; Figure 6; and Figure 7);

e. A hardware resource for carrying out a process for updating said program counter among processes which take place in the course of execution of said specific

instruction (Applicant's claim 9) (Levy column 5, lines 18-42; column 7, lines 29-42; column 9, lines 42-46; Figure 3; Figure 6; and Figure 7); and

f. A status register for holding information indicative of a need of said notification and wherein said main processor periodically accesses said status register to recognize, from content of said status register, that said co-processor has encountered said specific instruction to thereby execute said specific instruction (Applicant's claim 10) (Levy column 5, lines 18-42; column 7, lines 29-64; column 8, lines 21-24; Figure 3; Figure 6; and Figure 7).

21. Referring to claims 12-16, Levy has taught

a. An instruction queue for holding a fetched instruction which belongs to said second instruction set (Applicant's claim 12) (Levy column 8, lines 34-41; column 9, lines 42-59; and Figure 3);

b. Wherein said main processor refers to said instruction queue of said co-processor to specify an interrupt handler which corresponds to said specific instruction to be executed (Applicant's claim 12) (Levy column 9, lines 42-59; Figure 6; and Figure 7);

c. Wherein said co-processor includes a stack architecture (Applicant's claim 13) (Levy Abstract; column 5, lines 31-59; and Figure 3);

d. A stack memory provided outside said co-processor (Applicant's claim 14) (Levy Abstract; column 7, lines 61-64; column 11, lines 1-14; and Figure 3),

e. A stack-top register for holding a predetermined number of top data of stack data (Applicant's claim 14) (Levy column 5, lines 18-42; column 7, lines 29-42; Figure 3; and Figures 8-12);

f. A cache memory provided between said stack memory and said stacktop register for caching a part of data held in said stack memory (Applicant's claim 15) (Levy column 11, lines 1-14; Figure 3; and Figure 10); and

g. Wherein said co-processor detects a predetermined instruction for which stack data needs to be manipulated over said stack-top register and said stack memory (Applicant's claim 16) (Levy column 12, lines 1-43 and Figures 8-12),

h. Whereupon said co-processor moves contents of said stack-top register to said stack memory (Applicant's claim 16) (Levy column 12, lines 1-43 and Figures 8-12) and thereafter requests said main processor to execute said predetermined instruction (Applicant's claim 16) (Levy column 6, lines 50 to column 7, line 24), said main processor referring to contents of said stack memory, to which said contents of said stack-top register have been moved (Applicant's claim 16) (Levy column 12, lines 1-43 and Figures 8-12), to thereby execute said predetermined instruction (Applicant's claim 16) (Levy column 12, lines 1-43 and Figures 8-12). In regards to Levy, the example embodiment completes stack instructions in the co-processor, but, as is stated in column 6, line 50 to column 7, line 24 of Levy, the co-processor may send these instructions to the host.

22. Referring to claim 18, Levy has taught a program memory in which instructions belonging to said second instruction set are contained, wherein said co-processor further comprises:

a. A program counter for holding an address of an instruction that is currently processed and belongs to said second instruction set (Levy column 5, lines 8-42; column 7, lines 29-42; column 9, lines 42-46; Figure 3; Figure 6; and Figure 7);

b. An instruction queue for holding instructions which belong to said second instruction set (Levy column 8, lines 34-41; column 9, lines 42-59; and Figure 3); and

c. An instruction fetch circuit for fetching an instruction belonging to said second instruction set from said program memory using a value contained in said program counter as its address and for setting the fetched instruction to said instruction queue (Levy column 5, lines 8-42; column 7, lines 29-42; column 8, liens 34-41; column 9, lines 42-59; Figure 3; Figure 6; and Figure 7).

23. Referring to claims 25 and 27, Levy has taught

a. Wherein said co-processor issues said notification by dedicated interrupt assigned in advance respectively to a predetermined number of instructions among the instructions belonging to said second instruction set which have a higher frequency of execution than the other instructions (Applicant's claim 25) (Levy Abstract; column 6, line 50 to column 7, line 24; Figure 6; and Figure 7).

b. Wherein said main processor comprises an interrupt request reception circuit for encoding said dedicated interrupt sent form said co-processor (Applicant's claim

27) (Levy column 8, lines 21-24; column 9, lines 46-59; column 10, lines 4-36; Figure 3; Figure 6; and Figure 7).

24. Levy has not taught

a. Interrupt vectors (Applicant's claims 25 and 27); and

b. To specify an interrupt handler which corresponds to said specific instruction to be processed (Applicant's claim 27).

25. Holmbo has taught

a. Interrupt vectors (Applicant's claims 25 and 27) (Holmbo Abstract; column 2, lines 11-21 and 43-58; column 3, lines 4-8, 30-43, and 60-67; and Figure 2); and

b. To specify an interrupt handler which corresponds to said specific instruction to be processed (Applicant's claim 27) (Holmbo Abstract; column 2, lines 11-21 and 43-58; column 3, lines 4-8, 30-43, and 60-67; and Figure 2).

26. A person of ordinary skill in the art at the time the invention was made, and as taught by Holmbo, would have recognized that using vector interrupts decreases the delay caused by executing an interrupt (Holmbo column 2, lines 6-8), thereby increasing the speed and efficiency of interrupt execution. In regards to Holmbo, Holmbo has taught in the cited lines that executing an interrupt in the additional peripheral device that does not use interrupt vectors like the processor in Holmbo's device causes a delay in executing the interrupt routine. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the interrupt vectors of Holmbo in the device of Levy to increase the speed and efficiency of interrupt execution.

27. Referring to claims 30 and 32, Levy has taught

a. Wherein said co-processor includes a stack architecture (Applicant's claim 30) (Levy Abstract; column 5, lines 31-59; and Figure 3);

b. A stack-top register for holding a predetermined number of top data of stack data (Applicant's claim 32) (Levy column 5, lines 18-42; column 7, lines 29-42; Figure 3; and Figures 8-12); and

c. A cache memory provided between said stack memory and said stacktop register for caching a part of data held in said stack memory (Applicant's claim 32) (Levy column 11, lines 1-14; Figure 3; and Figure 10).

28. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Levy, U.S. Patent Number 5,923,892 (herein referred to as Levy) in view of Holmbo, U.S. Patent Number 4,860,200 (herein referred to as Holmbo), as applied to claim 2 above, and in further view of Irwin, U.S. Patent Number 4,695,945 (herein referred to as Irwin). Levy has not explicitly taught wherein said co-processor detects an encounter with a specific one of the instructions belonging to said second instruction set for which data presently under the control of said main processor needs to be handled to thereby determine that said co-processor has encountered a specific instruction which cannot be processed by itself. However, Levy has taught wherein said co-processor detects an encounter with a specific one of the instructions belonging to said second instruction set to thereby determine that said co-processor has encountered a specific instruction which cannot be processed by itself (Levy Abstract; column 9, lines 46-59; column 10, lines 4-36; Figure 2; Figure 3; Figure 6; and Figure 7). Irwin has taught wherein said co-processor detects an encounter with a specific one of the instructions belonging to said second instruction set for which data presently under the control of said main processor needs to be handled to

thereby determine that said co-processor has encountered a specific instruction which cannot be processed by itself (Irwin Abstract; column 2, lines 39-64). A person of ordinary skill in the art at the time the invention was made, and as stated in Irwin, would have recognized that detecting this type of encounter is necessary to identify possible problems of contention for system resources (Irwin column 2, lines 22-24). By identifying these encounters, the processors resolve the resource contention and allow for processing to continue. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the encounter detection of Irwin in the device of Levy to resolve resource contention.

29. Claims 17 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levy, U.S. Patent Number 5,923,892 (herein referred to as Levy) in view of Holmbo, U.S. Patent Number 4,860,200 (herein referred to as Holmbo), as applied to claim 1 above, and in further view of Yamanaka, U.S. Patent Number 4,774,625 (herein referred to as Yamanaka). Levy has not taught a plurality of coprocessors in correspondence with a plurality of processes described in a program. Yamanaka has taught a plurality of coprocessors in correspondence with a plurality of processes described in a program (Yamanaka column 1, line 21 to column 2, line 28; Figure 1; and Figure 2). A person of ordinary skill in the art at the time the invention was made would have recognized that the plurality of coprocessors would allow for more operations to be executed simultaneously, thereby increasing speed of the processor. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the plurality of coprocessors of Yamanaka in the device of Levy to increase processor speed.

30. Claim 33 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levy, U.S. Patent Number 5,923,892 (herein referred to as Levy), as applied to claims 24 and 26 above, in view of Yamanaka, U.S. Patent Number 4,774,625 (herein referred to as Yamanaka). Levy has not taught a plurality of coprocessors in correspondence with a plurality of processes described in a program. Yamanaka has taught a plurality of coprocessors in correspondence with a plurality of processes described in a program (Yamanaka column 1, line 21 to column 2, line 28; Figure 1; and Figure 2). A person of ordinary skill in the art at the time the invention was made would have recognized that the plurality of coprocessors would allow for more operations to be executed simultaneously, thereby increasing speed of the processor. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the plurality of coprocessors of Yamanaka in the device of Levy to increase processor speed.

Allowable Subject Matter

31. Claims 19-23 are allowed. The following is an examiner's statement of reasons for allowance: Independent claims 19 and 23 both contain the limitations

> ...said interrupt vector comprising a dedicated interrupt vector component and a common interrupt request component,
>
> said dedicated interrupt vector component comprising an encoding for a specific interrupt handler to be executed by said main processor and said common interrupt request component provides an indication for a request for one of a plurality of interrupt handlers to be specifically identified by additional information.

32. Prior art contains interrupts vectors that specify the interrupt handler to be executed, but not interrupt vectors that specify the interrupt handler to be executed and request another interrupt handler identified by other information.

33. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

34. Applicant's arguments with respect to claims 1-35 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

36. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

37. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
24 June 2005

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100